In the Claims:

1. (Currently Amended) A method for testing a radio frequency (RF) circuit comprising:

observing a signal from the RF circuit, wherein the signal is a digital signal from within a processing portion of the RF circuit, wherein the signal has a high degree of correlation with an RF output of the RF circuit, and wherein the observing occurs outside of the RF circuit;

manipulating the signal; and

producing a metric for the test based on results from the manipulating.

2. (Original) The method of claim 1, wherein the testing is performed using built-in self test (BIST) techniques.

3. (Original) The method of claim 1, wherein the signal is a phase error signal.

4. (Canceled)

5. (Currently Amended) The method of claim 3 [[4]], wherein a transfer function between the signal and the RF output phase is flat within a frequency band of interest.

6. (Original) The method of claim 1, wherein the RF circuit is an all-digital circuit, and wherein the signal is an output of a component in an all-digital phase-locked loop in the RF circuit.

7. (Original) The method of claim 6, wherein the signal is an output of a phase detector.

8. (Original) The method of claim 7, wherein the signal has been filtered.

9. (Original) The method of claim 8, wherein the all-digital phase-lock loop is operating in a type-II mode, and the signal is an output of an integral accumulator of a loop filter.

10. (Original) The method of claim 8, wherein the all-digital phase-lock loop is operating in a type-I mode, and the signal is an output of an infinite impulse response filter coupled to the output of a loop filter.

11. (Original) The method of claim 8, wherein a loop filter coupled to an output of a phase detector performs the filtering, and wherein the signal is an output of the loop filter.

12. (Original) The method of claim 6, wherein the signal is an output of a gain normalization block.

13. (Original) The method of claim 1, wherein the frequency of the signal is several orders of magnitude less than the frequency of the RF output.

14. (Original) The method of claim 1, wherein the test is for phase error trajectory and the signal is the output of a phase detector, and wherein the manipulation comprises measuring a change in the signal.

15. (Original) The method of claim 14, wherein if the change in the signal is less than a specified threshold, then the phase error trajectory is good.

16. (Original) The method of claim 14, wherein the measuring the change in the signal comprises measuring a peak, a variance, or a rate of change in the signal.

17. (Original) The method of claim 1, wherein the test is for frequency lock and the signal is the output of a phase detector, and wherein the manipulation comprises comparing a value of the signal over several samples.

18. (Original) The method of claim 17, wherein if a variance in the magnitude is less than a specified threshold, then the frequency has been locked.

19. (Original) The method of claim 17, wherein the samples are taken at different times.

20. (Original) The method of claim 1, wherein the test is for frequency deviation and the signal is an output of an integral accumulator of a loop filter, and wherein the manipulation comprises comparing the signal with a specified range.

21. (Original) The method of claim 20, wherein if the signal is within the specified range, then the frequency deviation is within acceptable limits.

22. (Original) The method of claim 20, wherein the manipulation further comprises comparing several samples of the signal.

23. (Original) The method of claim 20, wherein the RF circuit contains an all-digital phase-locked loop operating in a type-II mode.

24. (Original) The method of claim 1, wherein the RF circuit contains an all-digital phase-locked loop, and the method further comprises prior to the observing, setting the all-digital phase-locked loop to a certain bandwidth.

25. (Original) The method of claim 24, wherein the test is for estimating phase noise power and the signal is an output of a phase detector, and wherein the manipulating comprises calculating a mean square error of the signal.

26. (Original) The method of claim 25, wherein the setting, observing, and manipulating is repeated for several different all-digital phase-locked loop bandwidths, and wherein the producing comprises subtracting the calculated mean square errors for the several different all-digital phase-lock loop bandwidths.

27. (Original) The method of claim 1, wherein the RF circuit is an all-digital frequency synthesizer.

28. (Original) The method of claim 1, wherein the RF circuit is an all-digital transmitter.

29. (Original) The method of claim 28, wherein the transmitter is used in a wireless communications network.

30. (Original) The method of claim 29, wherein the wireless communications network is Bluetooth compliant.

31. (Original) The method of claim 1, wherein the testing comprises a functional test or a compliance test of the RF circuit.

32. (Original) A circuit comprising:

a processor coupled to a radio frequency (RF) circuit, the processor containing circuitry to manipulate digital signals from the RF circuit to provide a performance metric for the RF circuit; and

a control signal input coupled to the processor, wherein the control signal input can enable an observation and manipulation of the digital signals.

33. (Original) The circuit of claim 32 further comprising a latch coupled to the processor, the latch to store the performance metric provided by the processor.

34. (Original) The circuit of claim 32, wherein the RF circuit is integrated onto a first integrated circuit, wherein the processor is integrated onto a second integrated circuit.

35. (Original) The circuit of claim 34, wherein the first and the second integrated circuits are the same integrated circuit.

36. (Original) The circuit of claim 32, wherein the RF circuit contains an all-digital phase-locked loop, and wherein the processor is coupled to an output of a phase detector.

37. (Original) The circuit of claim 32, wherein the RF circuit contains an all-digital phase-locked loop, and wherein the processor is coupled to a filtered output of a phase detector.

38. (Original) The circuit of claim 32, wherein the RF circuit contains an all-digital phase-locked loop, and wherein the processor is coupled to an output of a phase detector and a filtered output of a phase detector.

39. (Original) The circuit of claim 32, wherein the circuit permits the testing of the RF circuit in wafer, in packaged integrated circuit, in factory, and in field.

40. (Original) The circuit of claim 32, wherein the circuit permits the testing of the RF circuit, and wherein the testing is of a type selected from a group consisting of a phase trajectory error, a frequency lock, a frequency deviation, a phase noise power, or combinations thereof.

41. (Currently Amended) A circuit comprising:

a reference phase accumulator coupled to a signal input, the reference phase accumulator containing circuitry to compute a reference phase;

a phase detector coupled to the reference phase accumulator, the phase detector containing circuitry to compute a difference between the reference phase and a variable phase;

a digitally-controlled oscillator (DCO) coupled to the phase detector, wherein the performance of the DCO can be ascertained by a test circuit observing an output of the phase detector; and

a variable phase accumulator coupled to the DCO and the phase detector, the variable phase accumulator containing circuitry to compute the variable phase.

42. (Original) The circuit of claim 41 further comprising a time-to-digital converter (TDC) coupled to the DCO and the phase detector, the TDC containing circuitry to compute a time difference between a reference clock and a variable clock.

43. (Original) The circuit of claim 41 further comprising a loop filter coupled to the phase detector and the DCO, the loop filter to provide a desired amount of attenuation to the computed difference between the reference phase and the variable phase.

44. (Original) The circuit of claim 43, wherein the loop filter is of a type selected from a group consisting of a finite impulse response filter, an infinite impulse response filter or combination thereof.

45. (Original) The circuit of claim 44, wherein the loop filter is comprised of a plurality of filters, and wherein the filters are arranged in a parallel fashion.

46. (Original) The circuit of claim 44, wherein the loop filter is comprised of a plurality of filters, and wherein the filters are arranged in a cascaded fashion.

47. (Original) The circuit of claim 41 further comprising a gain normalization unit coupled to the phase detector and the DCO, the gain normalization unit to normalize the difference between the reference phase and the variable phase with respect to a gain in the DCO.